WHAT IS CLAIMED IS:

1. An encoder comprising:

filtering generation means which generates a filtering coefficient by performing a filtering processing on inputted picture data;

division means which divides the filtering coefficient into plural bit planes from an uppermost bit to a lowermost bit of each pixel;

read control means which removes a predetermined number of bit planes among the plural bit planes, from a lower side, thereafter reads remaining bit planes, and outputs the remaining bit planes in parallel; and

plural encoding means which respectively perform encoding processings on the plural bit planes outputted in parallel from the read control means, wherein

the read control means determines the number of the removed bit planes, so that a quantity of generated codes per frame is kept constant when each of the plural encoding means performs the encoding processing.

2. The encoder according to claim 1, wherein

the read control means removes the predetermined number of bit planes, from the lower side and from a lower hierarchical level, from bit planes stored in storage means.

3.   The encoder according to claim 1, further comprising

rate control means which performs feeding forward in order

that the quantity of generated codes per frame is kept constant,

based on results of the encoding processings of the plural encoding

means.

4.   An encoding method comprising:

a first step of generating a filtering coefficient by

performing a filtering processing on inputted picture data;

a second step of dividing the filtering coefficient into

plural bit planes from an uppermost bit to a lowermost bit of each

pixel;

a third step of removing a predetermined number of bit planes

among the plural bit planes, from a lower side, thereafter reading

remaining bit planes, and outputting the remaining bit planes in

parallel; and

a fourth step of performing encoding processings respectively

on the plural bit planes outputted in parallel, wherein

the number of the removed bit planes is determined in the

third step so that a quantity of generated codes per frame is kept

constant when the encoding processings are performed in the fourth

step.

5.   The method according to claim 4, wherein,

in the third step, the predetermined number of bit planes is

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removed from the bit planes, from the lower side and from a lower hierarchical level.

6.   The method according to claim 4, further comprising

a sixth step of setting the number of bit planes removed in the third step, which is necessary to keep the quantity of generated codes per frame constant, based on results of the encoding processings in the fourth step, and thereafter feeding back the number to the third step.